Amendments to the Claims:

1. (currently amended) An identification system comprising:

a reader including a transmitter for transmitting a reader signal; and

a plurality of transponders, each transponder including a counter, a receiver for receiving the reader signal and a transmitter for generating a response signal ~~continuing~~ containing data that ~~which~~ identifies the transponder, wherein at least one of the plurality of transponders is~~the transponder being~~ adapted to repeat the transmission of the response signal at intervals that ~~which~~ are random or pseudo-random in length and are based at least in part on a value of the counter that is generated when the reader signal is received. ~~characterised by a counter driven by a clock, the output from the counter providing a random number or providing a seed value for a random number generator to affect the randomness of the intervals between the response signals.~~

2. (currently amended) An identification system as claimed in claim 1, wherein the counter is ~~and the clock are~~ reset upon activation of a POWER-ON-RESET (POR) circuit.

3. (currently amended) An identification system as claimed in claim 1, wherein the counter ~~and clock~~ is part of an RFID ~~chip~~ transponder integrated circuit.

4. (currently amended) A transponder comprising:

a counter;

a receiver ~~means for receiving~~ configured to receive a reader signal; and[[,]]

~~transmission mans for transmitting~~ a transmitter configured to transmit a response signal containing data that ~~which~~ identifies the transponder, the transponder being adapted to repeat the transmission of the response signal at intervals that ~~which~~ are random or pseudo-random in length and are based at least in part on a value of the counter that is generated when the reader signal is received.[[,]] ~~characterised by a counter driven by a clock, the output from the counter providing a random number or providing a seed value for a random number generator to affect the randomness of the intervals between the response signals.~~

5. (currently amended) A transponder as claimed in claim 4, wherein the counter is ~~and the clock are~~ reset upon activation of a POWER-ON-RESET (POR) circuit.

6. (currently amended) An integrated circuit for use in a transponder, comprising:

a counter;

a receiver ~~means for receiving~~ configured to receive a reader signal; and[[,]]

~~transmission mans for transmitting~~ a transmitter configured to transmit a response signal containing data that ~~which~~ identifies the transponder, the integrated circuit being adapted to repeat the transmission of the response signal at intervals that ~~which~~ are random or pseudo-random in length and are based at least in part on a value of the counter that is generated when the reader signal is received.[[,]] ~~characterised by a counter driven by a clock, the output from the counter providing a random number or providing a seed value for a random number generator to affect the randomness of the intervals between the response signals.~~

7. (currently amended) An integrated circuit as claimed in claim 6, wherein the counter is ~~and the clock are~~ reset upon activation of a POWER-ON-RESET (POR) circuit.

8. (previously presented) An integrated circuit as claimed in claim 7, wherein the integrated circuit is part of an RFID ~~chip~~ transponder integrated circuit.

9. (currently amended) A method of identifying a plurality of transponders, comprising:

exposing a transponder to RF whereby a capacitor is charged to a predetermined value to activate a POWER-ON-RESET (POR) circuit, wherein the transponder is adapted to transmit a response signal containing data that identifies the transponder, and wherein the transponder comprises a counter driven by a clock that is responsive to activation of the POR circuit; and

exposing the transponder to ~~the transponder being responsive to~~ a command signal from a reader to cause or repeat the transmission of the [[a]] response signal~~, containing data which identifies the transponder,~~ at intervals that ~~which~~ are random or pseudo-random in length and are

based at least in part on a value of the counter that is generated when the command signal is received from the reader.[[,]] ~~characterised by a counter driven by a clock responsive to activation of the POR to provide an output signal when the command signal has been received, the output signal providing a random number or a seed for a random number generator, a slot selection or random transmit repeat (hold-off) value for the response signals being dependent directly or indirectly on said output signal.~~

10. (currently amended) An identification system as claimed in claim 1, wherein the counter is ~~and clock are~~ routed to a latch/transmit shift register such that when the reader signal ~~a command~~ is received by the transponder, the ~~instantaneous~~ value of the counter is stored in the latch/transmit shift register.

11. (currently amended) An identification system as claimed in claim 10, wherein the latch/transmit shift register provides a random number or a seed value for a random number generator to affect the randomness of the intervals between the response signals.

12. (currently amended) A transponder as claimed in claim 4, wherein the counter is ~~and clock are~~ routed to a latch/transmit shift register such that when the reader signal ~~a command~~ is received by the transponder, the ~~instantaneous~~ value of the counter is stored in the latch/transmit shift register.

13. (currently amended) A transponder as claimed in claim 12, wherein the latch/transmit shift register provides a random number or a seed value for a random number generator to affect the randomness of the intervals between the response signals.

14. (currently amended) An integrated circuit as claimed in claim 6, wherein the counter is ~~and clock are~~ routed to a latch/transmit shift register such that when the reader signal ~~a command~~ is received by the transponder, the ~~instantaneous~~ value of the counter is stored in the latch/transmit shift register.

15. (currently amended) An integrated circuit as claimed in claim 14, wherein the latch/transmit shift register provides a random number or a seed value for a random number generator to affect the randomness of the intervals between the response signals.

16. (new) An identification system comprising:

a reader including a transmitter for transmitting a reader signal; and

a plurality of transponders, each transponder including a counter driven by a clock, a receiver for receiving the reader signal and a transmitter for generating a response signal containing data that identifies the transponder, wherein at least one of the plurality of transponders is adapted to repeat the transmission of the response signal at intervals that are random or pseudo-random in length and are based at least in part on a value of the counter when the reader signal is received,

wherein the clock has a period, and

wherein the value of the counter is based at least in part on the period of the clock.

17. (new) An identification system as claimed in claim 16, wherein the counter is reset upon activation of a POWER-ON-RESET (POR) circuit.

18. (new) An identification system as claimed in claim 16, wherein the counter is part of an RFID transponder integrated circuit.

19. (new) An identification system as claimed in claim 16, wherein the counter is routed to a latch/transmit shift register such that when the reader signal is received by the transponder, the value of the counter is stored in the transmit shift register.

20. (new) An identification system as claimed in claim 19, wherein the latch/transmit shift register provides a random number or a seed value for a random number generator to affect the randomness of the intervals between the response signals.